Center for Integrated Space Microsystems (CISM)
A JPL Center of Excellence

Power Awareness in Deep Space Missions

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Outline

- Deep Space Missions at JPL
- The Needs for Power Awareness in Deep Space Missions
- Power System Design in Current Spacecraft Designs
- Recent Efforts in Power Awareness at JPL
  - Selection of IEEE 1394 Bus
  - Power Management Features in Power PC Processor for X2000
- Hidden Issues in Power Awareness
  - Fault Tolerance
  - Cost of Power Management

Outline, continued

- Next Generation Power Awareness Design
  - X2000 Future Deliveries
  - SOAC
  - E.H.?
- Advanced Power Awareness Research at JPL
  - University of Notre Dame
  - University of California, Irvine

Deep Space Missions at JPL

Mission	Launch Date	Power Budget	Distance from Sun	Energy from Sun (Compare to Earth)
Pluto/Kuiper Express	2004	?	39.5 AU	0.0006
Europa Orbiter	2006	?	5.2 AU	0.0370
Europa Lander	TBD	TBD	5.2 AU	0.0370
Saturn Ring Observer	TBD	TBD	9.5 AU	0.0109
Titan Organic Explorer	TBD	TBD	9.5 AU	0.0109

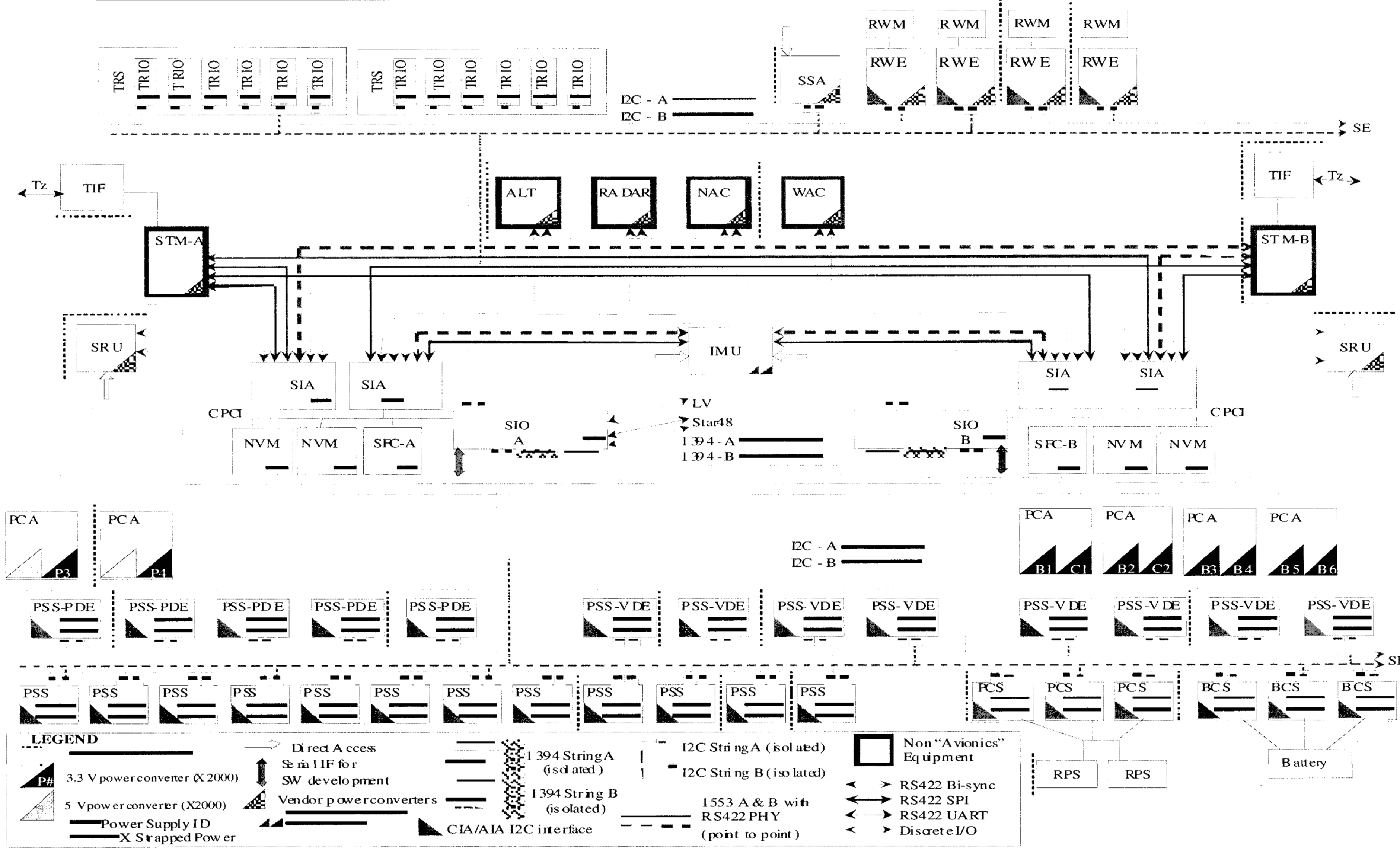
The Needs for Power Awareness in Deep Space Missions

- Power is always a premium resource for deep space missions
- Solar power is not practical for deep space missions: outer planets receive only a few percent of the solar energy as on Earth
- Nuclear power is necessary but not political viable
- Need to reduce power consumption to cut down radioactive materials on-board

Power System Design in Current Spacecraft Designs

- Europa Orbiter and Pluto/Kuiper Express Power System Design
  - Primary power switching (28 V), power conversion (3.3 V and 5 V) at the loads
  - Power switches are centralized
  - Power switches are grouped in slices, 4 switches/slice
  - Power switch slice has smart interface to communicate with Flight Computer
  - Flight Computer commands the power switches via I^2C bus

EO Avionics Block Diagram



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Recent Efforts in Power Awareness at JPL

- Impact of power awareness in X2000 architecture
  - A dual bus architecture to satisfy both high performance and low power requirement
  - Selection of IEEE 1394 Bus instead of 1553 or Fiber Channel
  - Selection of I2C bus instead of CAN and other engineering bus
  - Functional redundancy instead of block redundancy

- Power management features of Power PC processor in X2000
  - Need Dwight's input

Hidden Issues in Power Awareness

- Fault tolerance
  - –Fault tolerance requires redundancy
  - –Redundancy requires additional power
  - –Need to manage redundancy carefully to minimize power consumption
- Cost of Power Management
  - More refined power management requires more power switches
  - More power switches require more hardware and control
  - For centralized power distribution architectures (e.g., Europa Orbiter and Pluto/Kuiper Express), more power switches require more wiring and bigger harness

Next Generation Power Awareness Design

- X2000 Future Delivery:
  - Distributed power management to reduce wiring complexity for power switching
- SOAC: A new paradigm needed because:
  - Power management by power switching is not practical for system-on-a-chip due to size of switches
  - Component modules are on the same chip and wiring complexity may not as serious as off-chip power distribution
  - On-chip power source may require different kind of power management and distribution scheme
- E.H.
  - (Leon, I forget what this is.)

Advanced Research in Power Awareness at JPL

- University of Notre Dame
  - Need to work with Benny and Mohammad
- University of California, Irvine
  - Need inputs

High-Level Plans: I, Study/Analysis

* DARPA Deliverables, ** Possible deliverables for future

- Analyze power consumption results from the JPL systems testbed measurements done on real systems for power management

- Prepare a report on the power consumption by systems components under various load conditions and application runs

- Study real JPL applications to determine the power optimization strategy in both H/W and S/W

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High-Level Plans: I Study/Analysis, Continued

- Survey H/W power optimization techniques used by industry in the
embedded microprocessors in palm top and notebook computers

- Analyze power management techniques implemented in the
- commercial power PC 750 and its Radhard (Lockheed Martin) version

- Periodic reporting and final reports. Publications.

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High-Level Plans: II
Measurements/Experiments

Configure a breadboard computing node using the PPC 750 for real measurement in the JPL testbed using real S/W and applications

- Present design modifications at the micro-architecture level of a microprocessor used as a computing unit in real systems. e.g.
    - Enhanced pipeline design
    - Enhanced super scaling
    - Pipeline gating
    - Clock distribution control
    - Optimum cache utilization and control
- Design a real time dynamic power management unit (ASI C) for external control.

High-level plans: II Measurements/Experiments, Continued

- *Implement H/W and S/W power optimization techniques to determine best strategies for power aware system architecture

  - S/W power optimization will include:
    - Instruction optimization
    - Application specific compiler optimization etc.

- Formulate dynamic power optimization techniques for one level higher system: e.g. avionics and finally the spacecraft.

- Determine similar techniques for the SOAC type integrated system designs

Architectures task: Update Collaboration with Univ. of Illinois - ECE

- <u>Professors contacted for collaboration in the ECE Dept.</u>
  - Janak Patel, Computer Architectures, Digital Testing Algorithms/Verification
  - Elizabeth Rudnick, Test Generation Fault Simulation Design for Testability
  - Naresh Shanbaug, Power optimization in Analog and mixed mode designs, DSP
  - Wen-mei W. Hwu, Computer architectures, Compilers
  - Sanjay Patel, High performance computer systems, architectures for dynamic program optimization,
    The microarchitecture of superscalar microprocessors,
    Instruction supply mechanisms for wide issue machines,
    Trace Caches.

Sanjay's - Publications

- Sanjay J. Patel and Steven S. Lumetta
  "rePLay : a Hardware Framework for Dynamic Program Optimization,"
  University of Illinois Technical Report, CRHC-99-16, December 1999.

- Sanjay J. Patel
  "Trace Cache Design for Wide-Issue Superscalar Processors,"
  PhD Dissertation, 1999, University of Michigan, Ann Arbor.

- Sanjay J. Patel, Daniel H. Friendly, and Yale N. Patt,
  "Evaluation of Design Options for the Trace Cache Fetch Mechanism,"
  IEEE Transactions on Computers, Feb 1999, Special Issue on Cache Memory and Related Problems.

- Daniel H. Friendly, Sanjay J. Patel, and Yale N. Patt,
  "Putting the Fill Unit to Work: Dynamic Optimizations for Trace Cache Microprocessors,"
  Proceedings of the 31st ACM/IEEE International Symposium on Microarchitecture, Dallas, TX, Dec 1998

- Marius Evers, Sanjay J. Patel, and Yale N. Patt,
  "An Analysis of Correlation and Predictability: What Makes Two-Level Branch Predictors Work,"
  Proceedings of the 25th International Symposium on Computer Architecture, Barcelona, Spain, June 1998

- Sanjay J. Patel, Marius Evers, and Yale N. Patt,
  "Improving Trace Cache Effectiveness with Branch Promotion and Trace Packing,"
  Proceedings of the 25th International Symposium on Computer Architecture, Barcelona, Spain, June 1998

- Daniel H. Friendly, Sanjay J. Patel, and Yale N. Patt,
  "Alternative Fetch and Issue Policies for the Trace Cache Fetch Mechanism,"
  Proceedings of the 30th ACM/IEEE International Symposium on Microarchitecture, Research Triangle Park, North Carolina, November, 1997.

Sanjay's - Publications, Continued

•Yale N. Patt, Sanjay J. Patel, Marius Evers, Daniel H. Friendly, and Jared Stark,"
"One Billion Transistors, One Uniprocessor, One Chip,"
IEEE Computer, September, 1997.

•Sanjay J. Patel, Daniel H. Friendly, and Yale N. Patt,
"Critical Issues Regarding the Trace Cache Fetch Mechanism,"
University of Michigan, Technical Report, CSE-TR-335-97, May, 1997.

Teaching Interests:

Freshman Computing: **Introduction to Computing Systems: From Bits and Gates to C and Beyond**

ECE 312: **Computer Organization and Design**

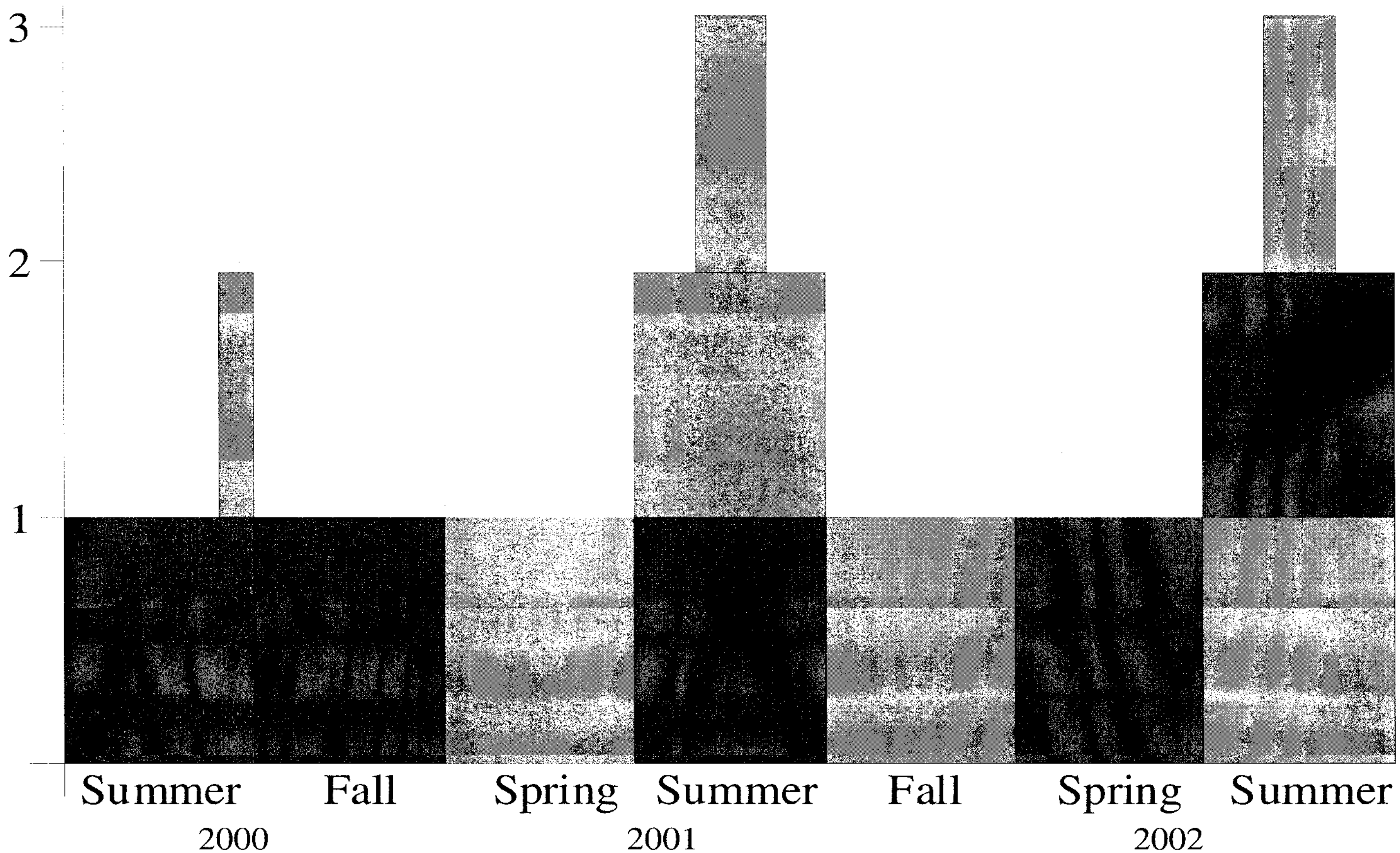
Students:

1. Brian: finishing undergraduate degree in January 2001
   will be a graduate student for Ph.D

2. Jeff: finishing MS in ECE in December 2000

3. Two more students are preparing to join in September 2000.

U of I personnel at the JPL:



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IMPAC^{2}T – Integrated Management of Power Aware Computation and Communication Technologies

- A collaboration effort - University of California - Irvine, JPL and USC
- An integrated CAD framework to study the overall architecture, interconnect requirements, and fault-tolerant properties of a large-scale, widely distributed, data acquisition system subject to hostile conditions.
- IMPAC^{2}T, explores the system architectures and communication strategies required to manage power most effectively in the presence of dynamic mission planning and replanning.
- Empowers system-level design in ways analogous to compilers for high-level programming languages. We envision that the designer uses these tools to instantiate and compose components, simulate and analyze the system with different power management policies, and synthesize and evaluate the power management mechanisms, which consist of a mix of hardware controllers and software schedulers.

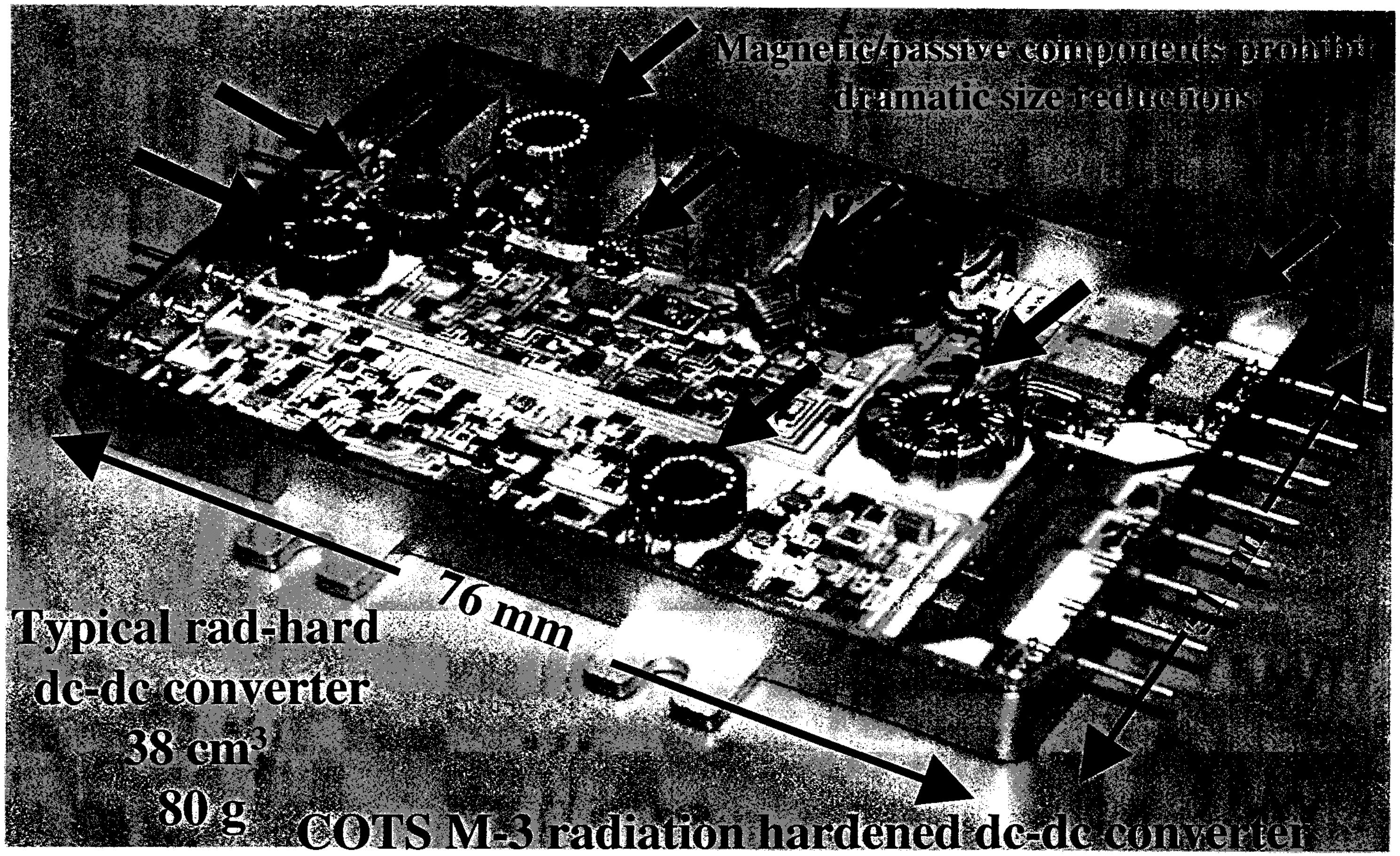
JPL Effort

- JPL shall investigate the feasibility and advantages of using IMPAC^{2}T tools to support complex real-time control tasks and computation-intensive applications for space missions.

- System Characterization and Architecture Definition:
  - Characterize energy versus performance profiles for previous missions such as the Pathfinder Rover, as well as new missions such as X2000 and Europa.
  - Identify different scenarios for X2000 subsystems where power aware technologies can be the enabling technology.

- Benchmark and Validation:
  - Benchmark IMPAC^{2}T tools against the existing X2000 subsystems in terms of performance versus power consumption and power management.
  - JPL and UCI will demonstrate with a prototype design that IMPAC^{2}T tools will synthesize significantly lower power and higher performance electronics as compared to existing designs and systems while offering a greater degree of flexibility.

State-of-the-Art Technology



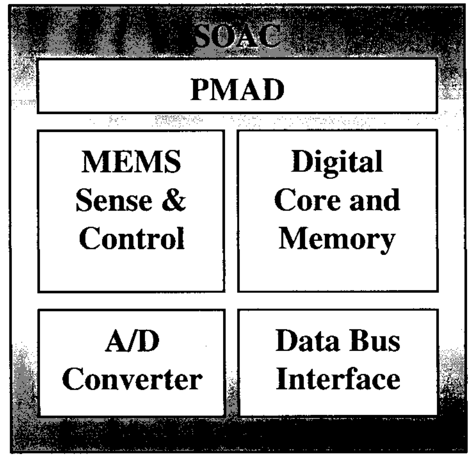
>200 Krad total dose tolerance

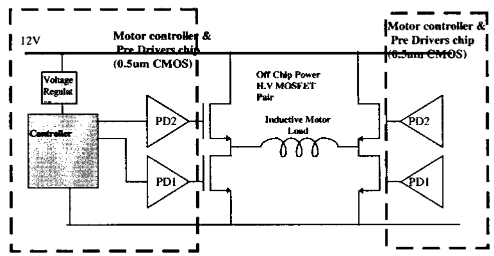
Efficiency = 82%

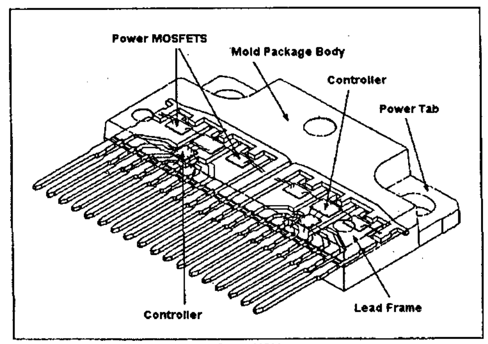
Power Density ≈ 11 mW/mm²

Program Goals

- The main goal of this program is to develop the a new revolutionary fully integrate on-chip power system for avionics SOAC with the following capabilities:
  - Provides high efficiency DC-DC voltage translation for the point of use
  - Uses on-chip embedded micro-passive elements for total integration
  - Directly plugs in to a single power bus
  - Self aware and provides adaptive power management







Power MCM.

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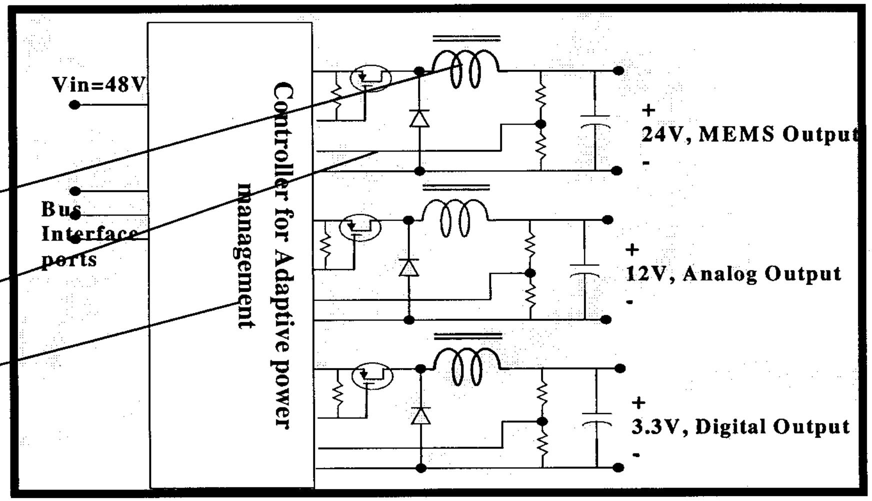
An Adaptive Multi Output Power Supply

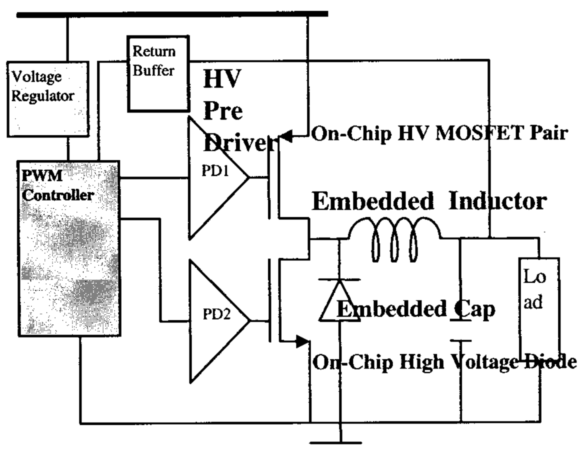


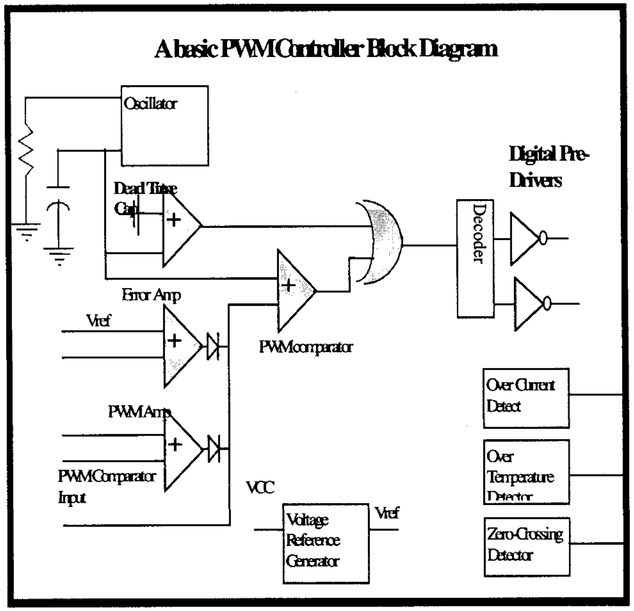
Description:
A high power high efficiency on chip multi output DC-DC power converter with bus interface and adaptive control

Needed Technologies

- **Embedded Passives**
- **High Voltage Devices in Sub-micron SOI CMOS**
- **Mixed Signal Sub-micron SOI Power Circuit and Sensors Library for Adaptive Control, Self Awareness & Digital Signal Processing**

28V **DC-DC Converter**





Cell Type	
Low Voltage	Precision References
Low Voltage	High-Speed Differential Input Amplifiers
Low Voltage	Comparators
Low Voltage	Operational Amplifiers
Low Voltage	Analog Buffers
Low Voltage	Oscillators
Low Voltage	Phase/Frequency Detectors
High Voltage	Rectifiers
High Voltage	Switching Inductor Drivers
High Voltage	Voltage Regulator
High Voltage	Analog Level Translator
High Voltage	Zero Crossing Detector
High Voltage	High Side Gate Pre-Driver

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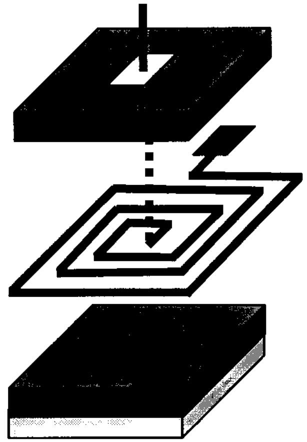
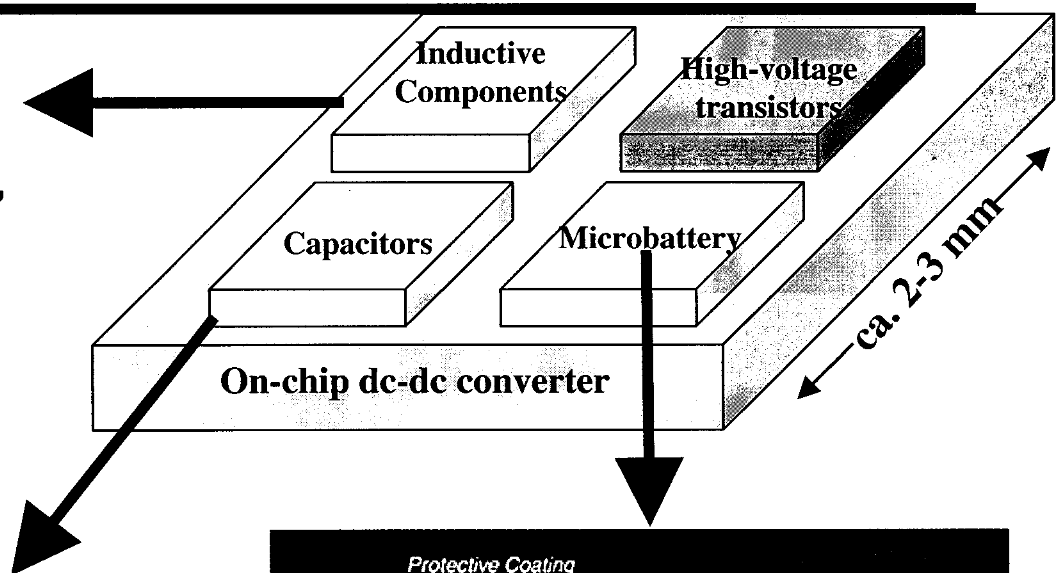
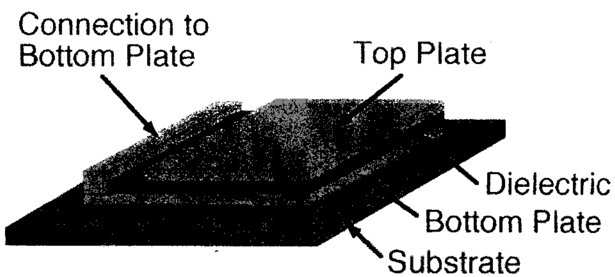
Passive Components: Keys to Integrated Power Electronics

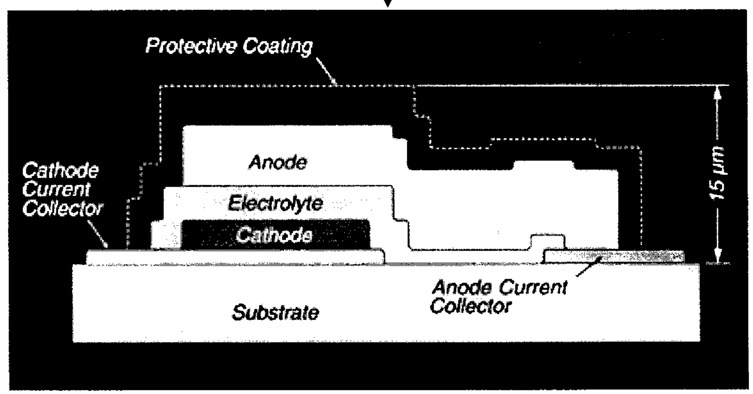
Magnetic thick film microinductors
CoZr or NiFe films
$>10\ \mu H/mm^2$
$Q > 10$
freq. = 1 MHz







Parallel Plate Capacitor
High dielectric capacitors
tantalum oxide or barium titanate films
$250\ nF/cm^2$ (800 Å thickness)
leakage limit of $1\ \mu A/cm^2$ at 10 V
effective series $R < 30\ m\Omega$



Rechargeable Li ion microbattery
3.5 V with tin oxide anode and solid electrolyte
$100\ \mu Ah/cm^2$ capacity
40,000 cycles
10-12 year lifetime

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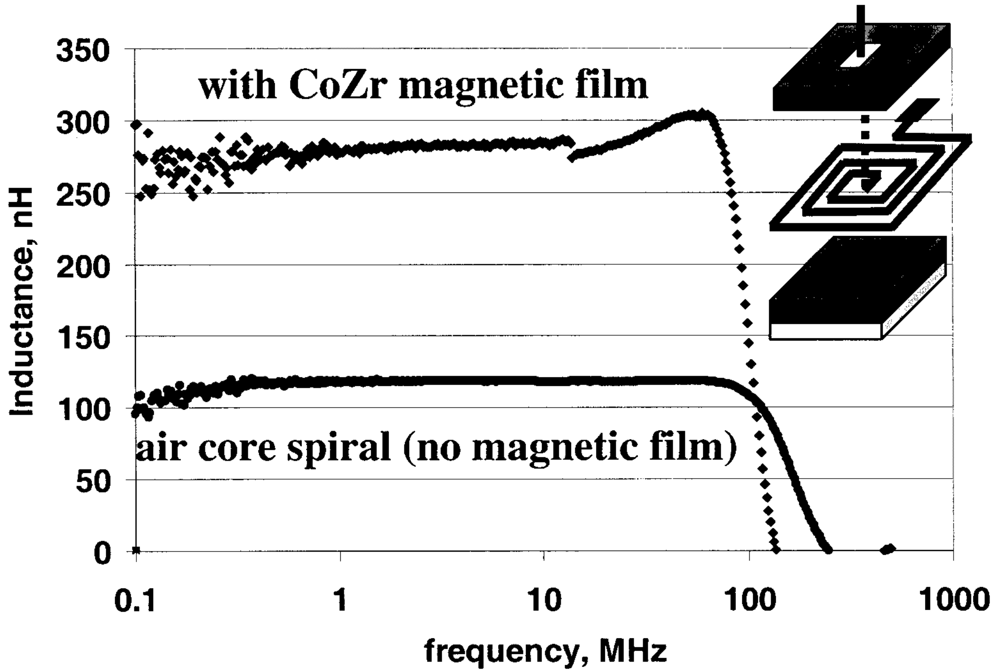
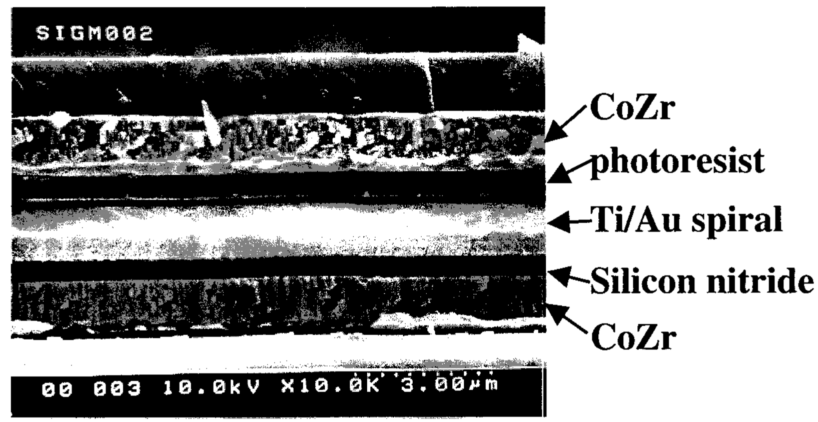
Integrated Microinductors Based on Magnetic Thick Films



Superior performance relative to air core

- frequency optimized for power (1 MHz)
- higher power handling capability
- higher inductance per unit area
- higher quality factor

For power applications: sandwich spiral inductor between thick, magnetic thin films to enhance inductance per unit area and Q



Cross Sectional SEM of Microinductor

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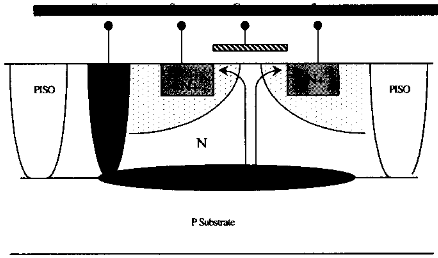
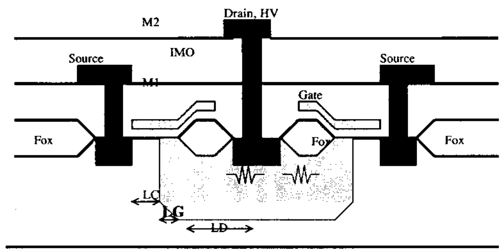
PowerAwarenessDARPA.ppt

A Rad-Hard SOI CMOS High Voltage Technology



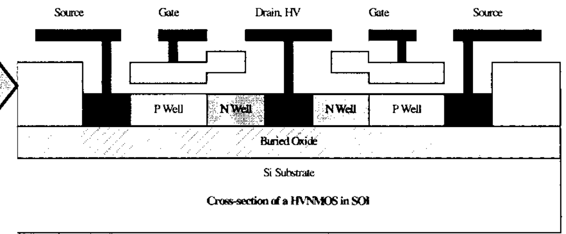
Cross Section of a DMOS in a Power CMOS process

HV Transistors in Power MOS Process



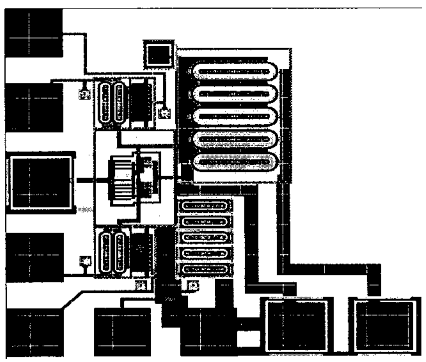
Cross-section of a HV NMOS in sub-micron VLSI bulk CMOS process

HV Transistors Compatible with VLSI CMOS Process

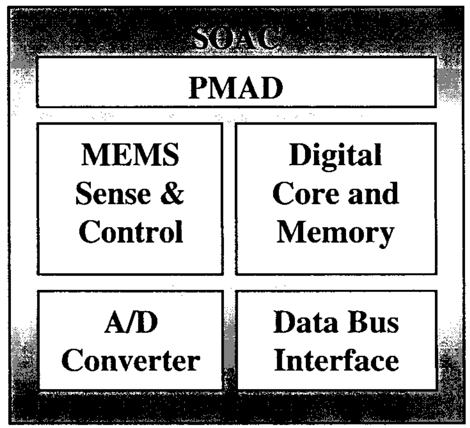


Cross-section of a HVNMOS in SOI

HV Transistors Compatible with SOI CMOS Process



30V Switching HV Driver Circuit



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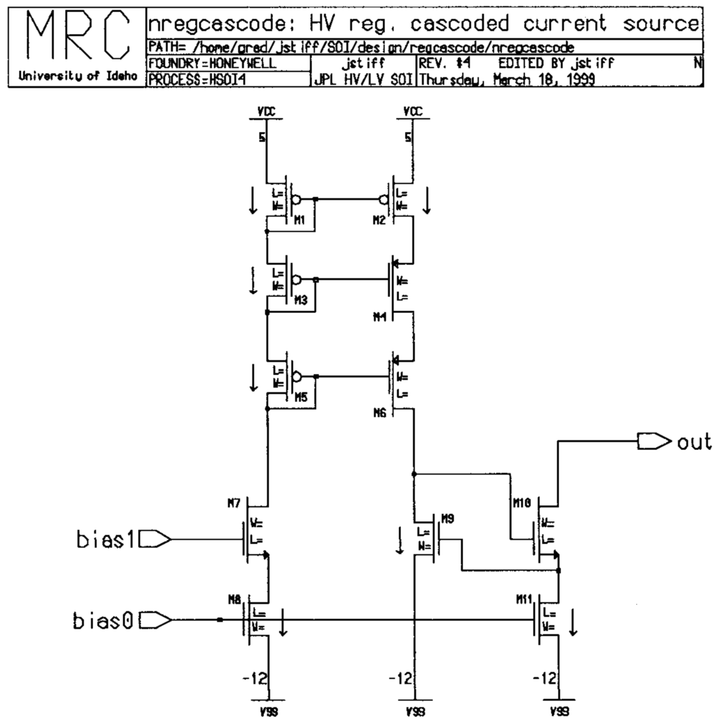
SOI CMOS Cell Library for PMAD

- Development of high-voltage analog circuits in SOI technology for PMAD.
  - Differential Amplifiers
  - Current Mirrors
  - Biasing Circuits
  - Bandgap Reference
  - OTA
  - Simple Op-Amp



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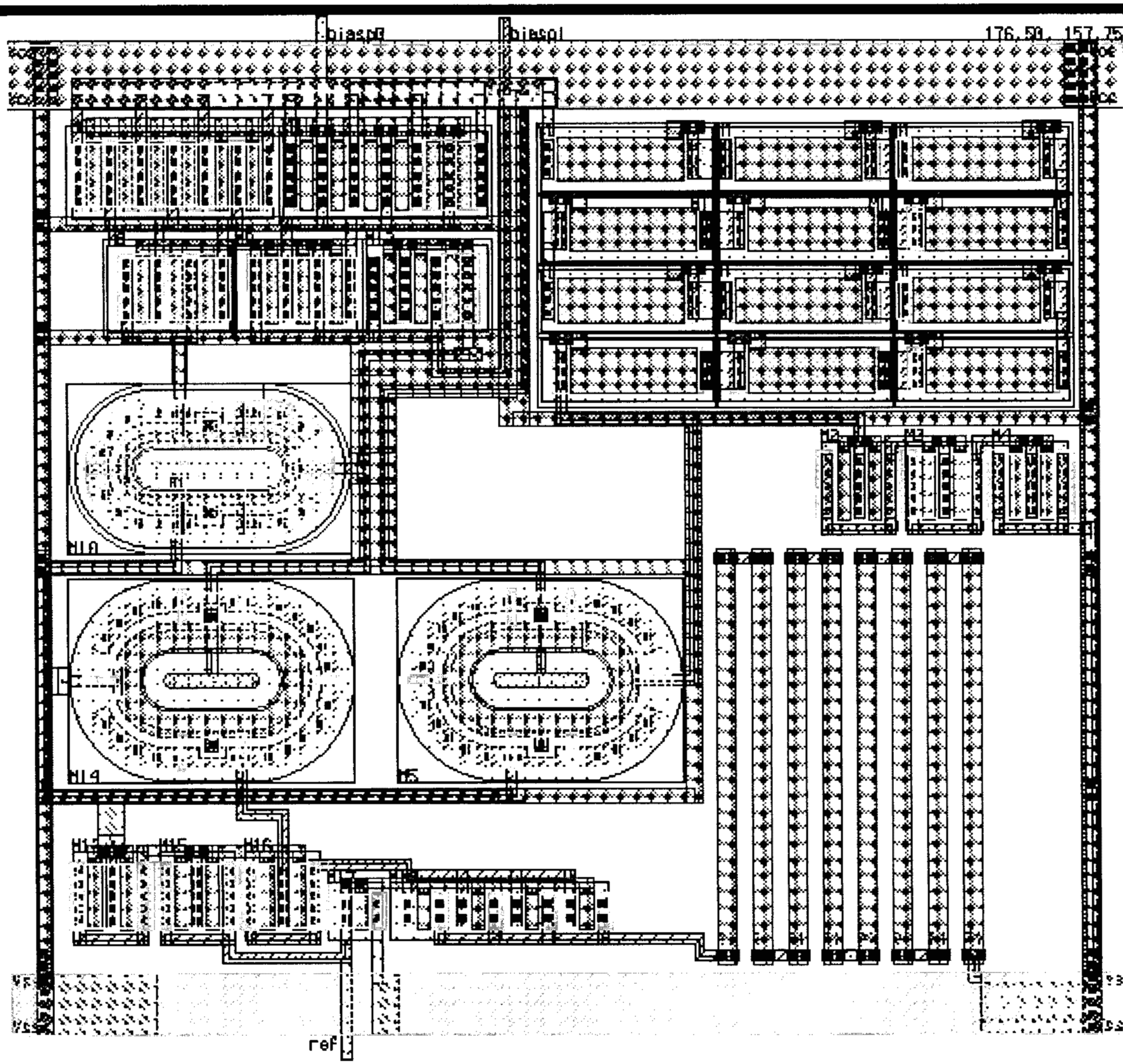
Beta-Multiplier Layout



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